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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,395	09/24/2003	Yee-Chia Yeo	TSM03-0511	3960

43859 7590 12/15/2005

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,395	YEO	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-47 and 58* is/are allowed.

6)☒ Claim(s) *48-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/27/05 has been entered. An action on the RCE follows.

a. The amendment filed on 10/27/2005 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 48, 50-52 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Yu et al. US patent No. 6,764,884.

Regarding claim 48, Inaba teaches (fig. 6) a method of forming a semiconductor device, the method comprising: providing a silicon substrate (11); etching portions of the silicon substrate to form at least one semiconductor fin (substrate projection region, 11a); forming a gate dielectric layer (13) over the semiconductor fin; forming a gate electrode (14) layer over the gate dielectric layer; etching portions of the gate electrode layer to form a gate electrode, the gate electrode overlying sidewalls and a top surface

of the semiconductor fin (refer to figs. 6 and 9); and doping the sidewall of the semiconductor fin above the region of material (also refer col. 8, lines 58-67 and col. 9, lines 1-12).

Inaba does not teach forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region of material.

The use of dielectric layer adjacent portions of the semiconductor fin not underlying the gate to protect the fin region from source/drain implantation is conventional in the art and also taught by Yu in the fabrication of a finfet structure using spacer regions (410) as shown in fig. 4 in the process of making source/drain region (col. 4, lines 40-47).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of spacer masking as taught by Yu in the process of Inaba in order to protect the region below the source/drain region from ion implantation. The combined process of Inaba and Yu would have a sidewall of the semiconductor fin extending above an upper surface of the region of material.

Regarding claim 50, Inaba teaches the entire claimed process of claim 48 above including forming a masking material over the silicon substrate and wherein the step of etching portions of the silicon substrate is performed in alignment with the masking material (col. 8, lines 58-67 and col. 9, lines 1-12).

Regarding claim 51, Inaba teaches the entire claimed process of claim 48 above including removing the masking material after the semiconductor fin is formed (col. 9, lines 1-12).

Regarding claim 52, Inaba teaches the entire claimed process of claim 48 above including the gate dielectric layer and the gate electrode layer are formed over the masking material (col. 8, lines 58-67 and col. 9, lines 1-12).

Regarding claim 55, Inaba teaches the entire claimed process of claim 48 above including forming an isolation region (12) adjacent the semiconductor region.

5. Claims 49 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, Yu and in view of Clark.

Regarding claims 49 and 53, Inaba teaches substantially the entire claimed method of claim 48 above except explicitly stating that the material comprises depositing a dielectric layer or depositing an oxide material.

It is conventional and also taught by Clark depositing dielectric layer.

It would have been obvious to one of ordinary skill in the art at the time invention was made to deposit the dielectric layer in the process of Inaba as taught by Clark in order to have better coverage. Since an oxide material is a dielectric material, it would have been obvious to one of ordinary skill in the art to deposit an oxide material in the process of Inaba as taught by Clark in order to get better oxide coverage.

6. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba, Yu et al. in view of Yu US patent No. 6,342,410.

Inaba teaches substantially the entire claimed method of claim 48 above except explicitly stating that the gate dielectric comprises a material with a relative permittivity greater than about 5.

Yu teaches the use of high permittivity gate dielectric material such as aluminum oxide with a dielectric constant of 8 in the process of forming a field effect transistor (col. 4, lines 36-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the permittivity material taught by Yu in the process of Inaba in order to minimize charge carrier tunneling through the gate dielectric.

Allowance

7. Claims 24-47 and 58 are allowed.

Response to Arguments

8. Applicant's arguments filed 10/27/05 have been fully considered but they are not persuasive. Applicant argues that the combination of Inaba and Yu (US. patent No. 6,764,884) does not or suggest the limitations of "forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface of the region material; and doping the sidewall of the semiconductor fin above the region of material" as recited in claim 48.

As stated above Inaba teaches substantially the entire claimed process of claim 48 except explicitly stating forming a region of material adjacent portions of the semiconductor fin not underlying the gate electrode such that a sidewall of the

semiconductor fin extends above an upper surface of the region of material. However Inaba teaches the formation of source/drain region above the bottom surface of the gate. Furthermore using of a dielectric mask to protect the fin region from source/drain implantation is conventional in the art and clearly Yu teaches (fig. 4 and col. 4, lines 40-47) the fabrication of a finfet structure using spacer regions (410) as shown in fig. 4 by forming a dielectric material that is later etched to form spacers (410), where the spacers are used to protect underlying regions of the fin 210 during the doping of the source/drain. Therefore the combined process of Inaba and Yu teaches the claimed process step as shown in the rejection above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 11, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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